



XJTAG – Transform Your PCBA Testing

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VP Regional Business Development

Fault Finding

Diagnosis

In-System Programming

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YOTTAVOLT



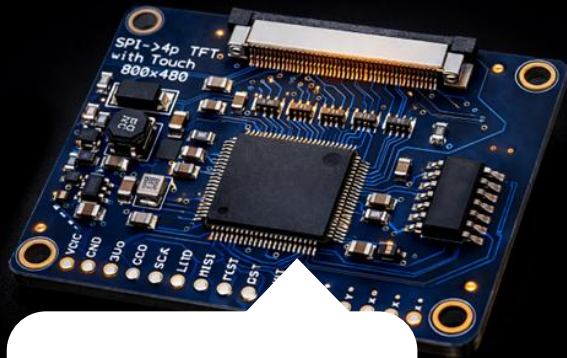


Electronics Trends

Why is Boundary Scan Becoming More Important Than Ever?

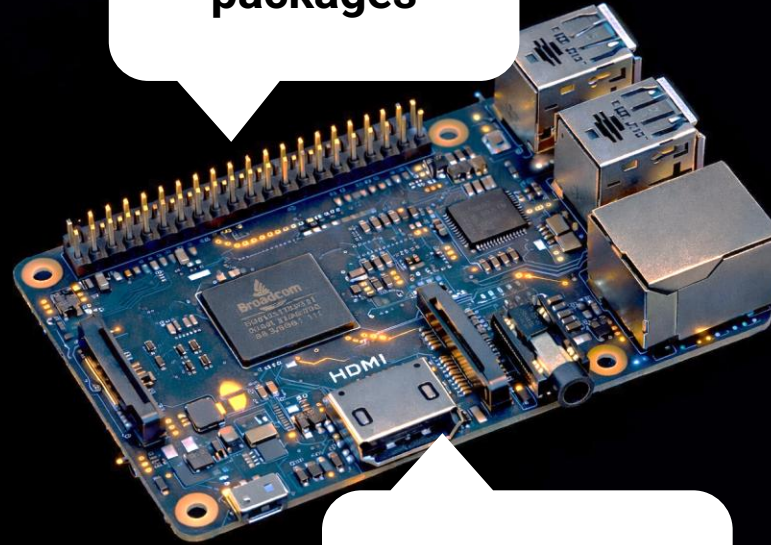
Electronics Complexity Is Growing

PCBAs



Test points and leads

Leadless packages



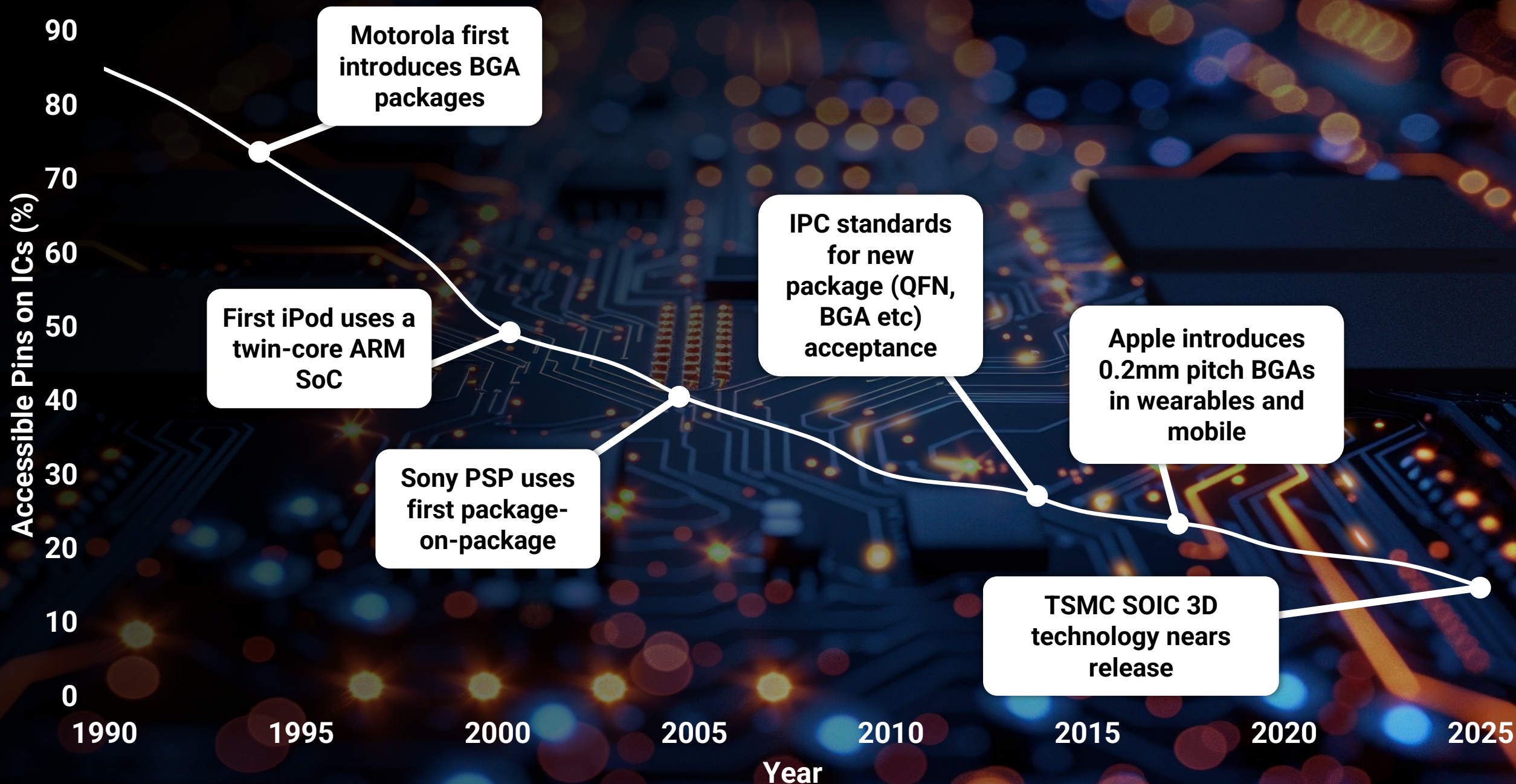
Headers and connectors

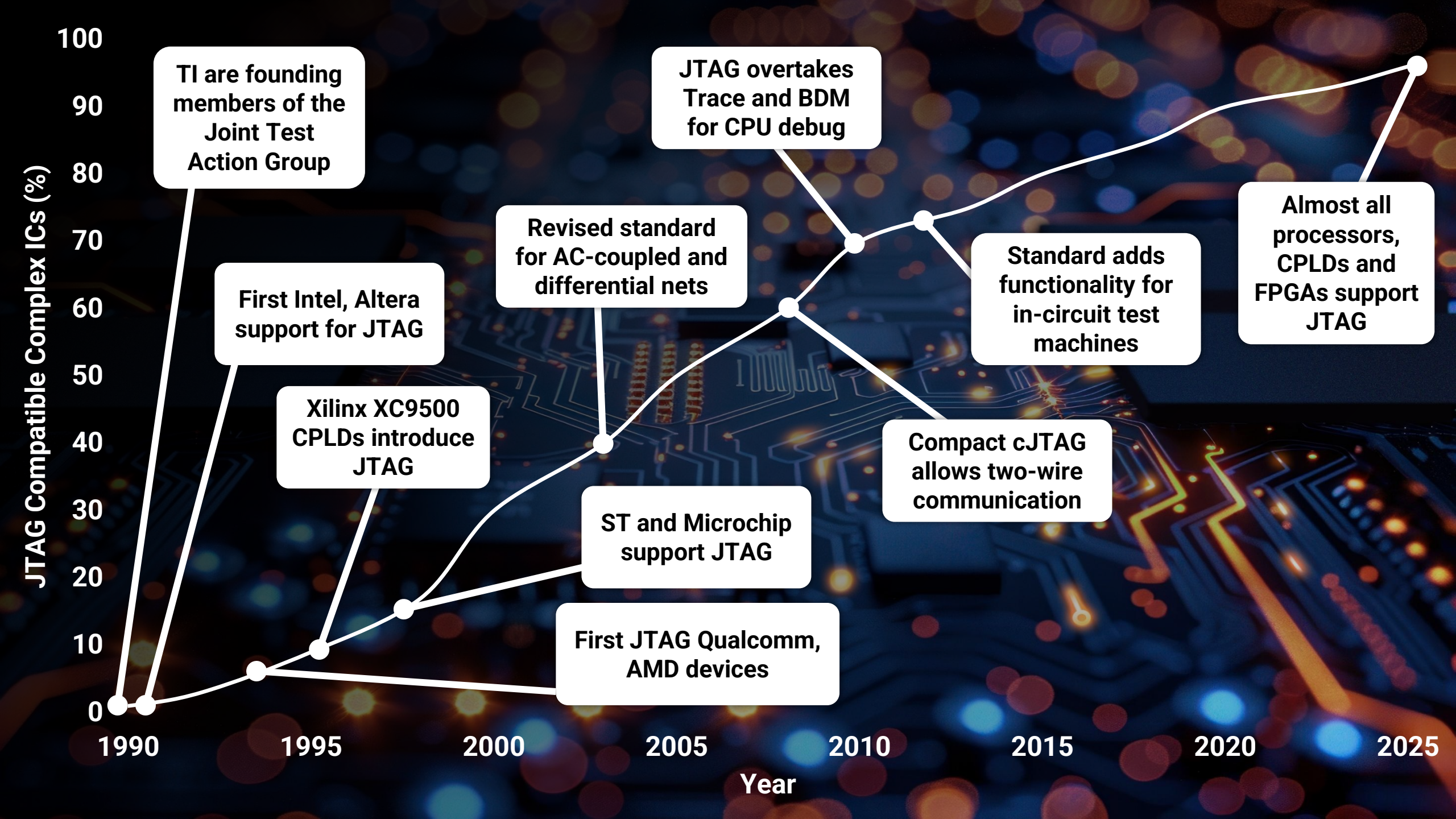
Systems-on-module



Minimal test access

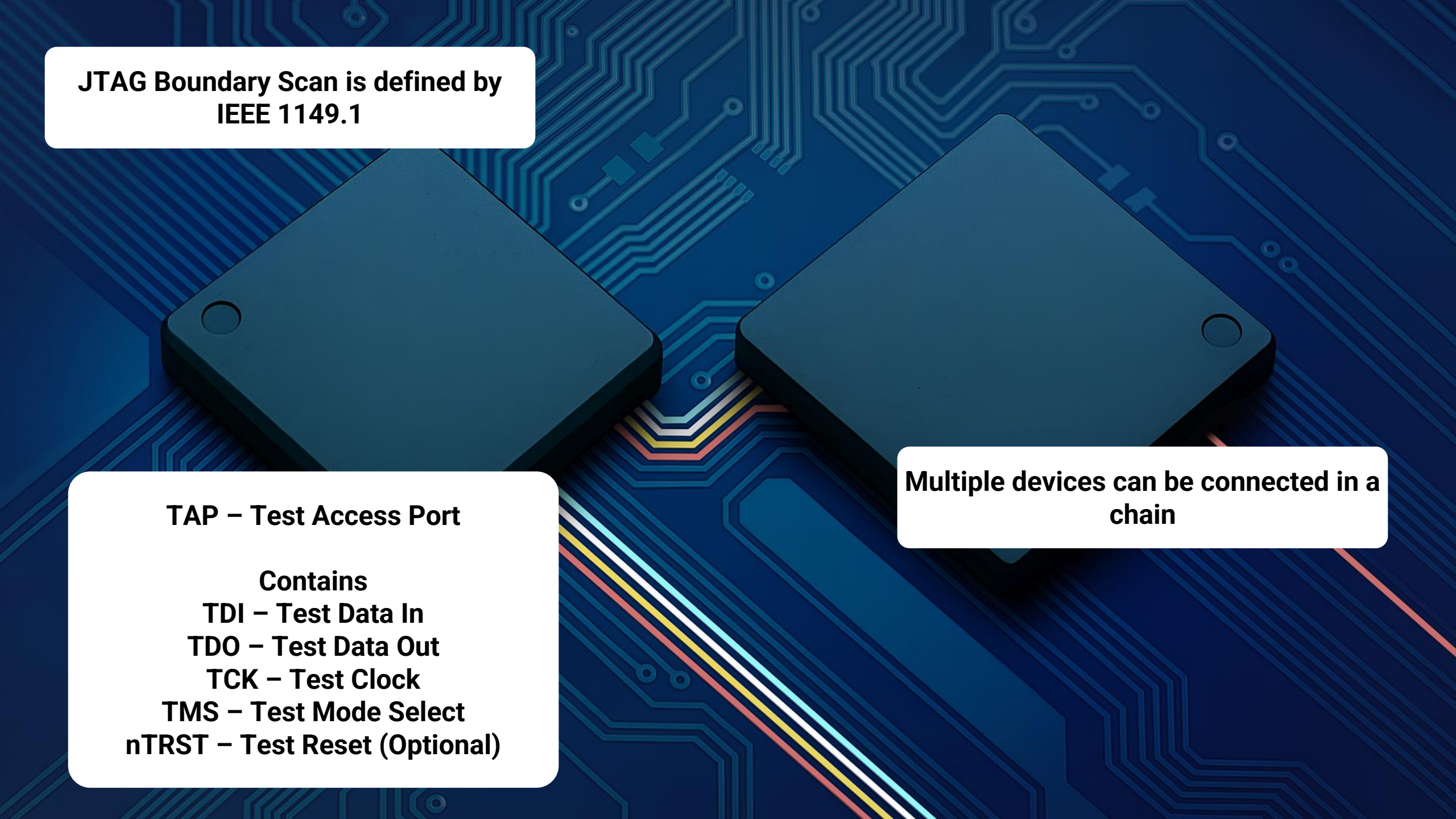
And Making Testing Harder





Technical Introduction

How Does JTAG Boundary Scan Work?



**JTAG Boundary Scan is defined by
IEEE 1149.1**

TAP – Test Access Port

Contains

TDI – Test Data In

TDO – Test Data Out

TCK – Test Clock

TMS – Test Mode Select

nTRST – Test Reset (Optional)

**Multiple devices can be connected in a
chain**



JTAG can access registers on the IC:

**Internal Registers
Bypass Register
Identification Register
Instruction Register**

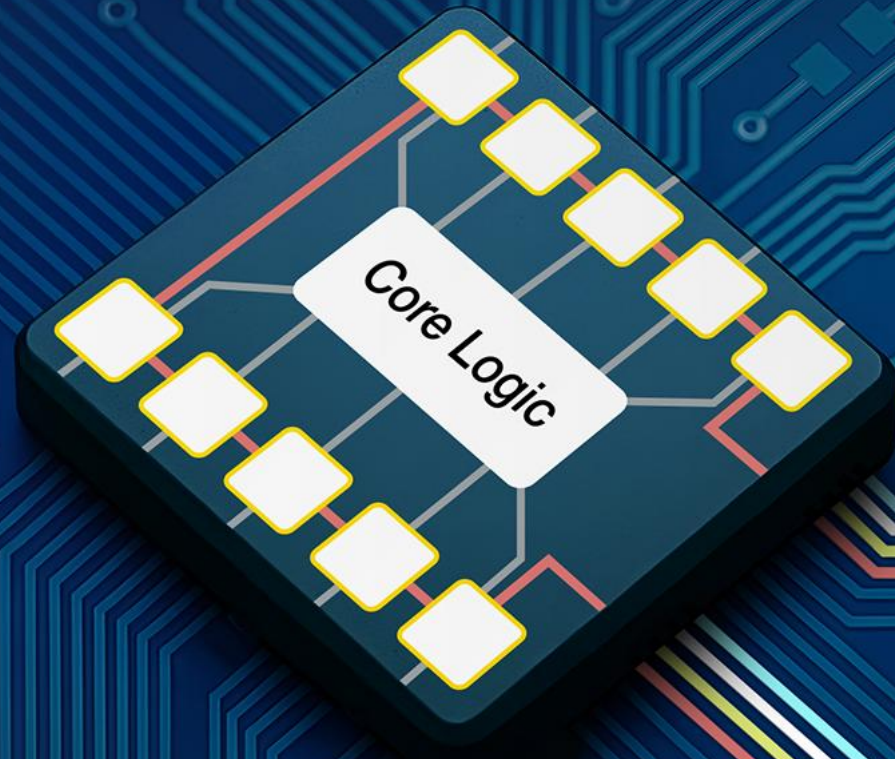
Each pin has a boundary scan cell. Each cell can:

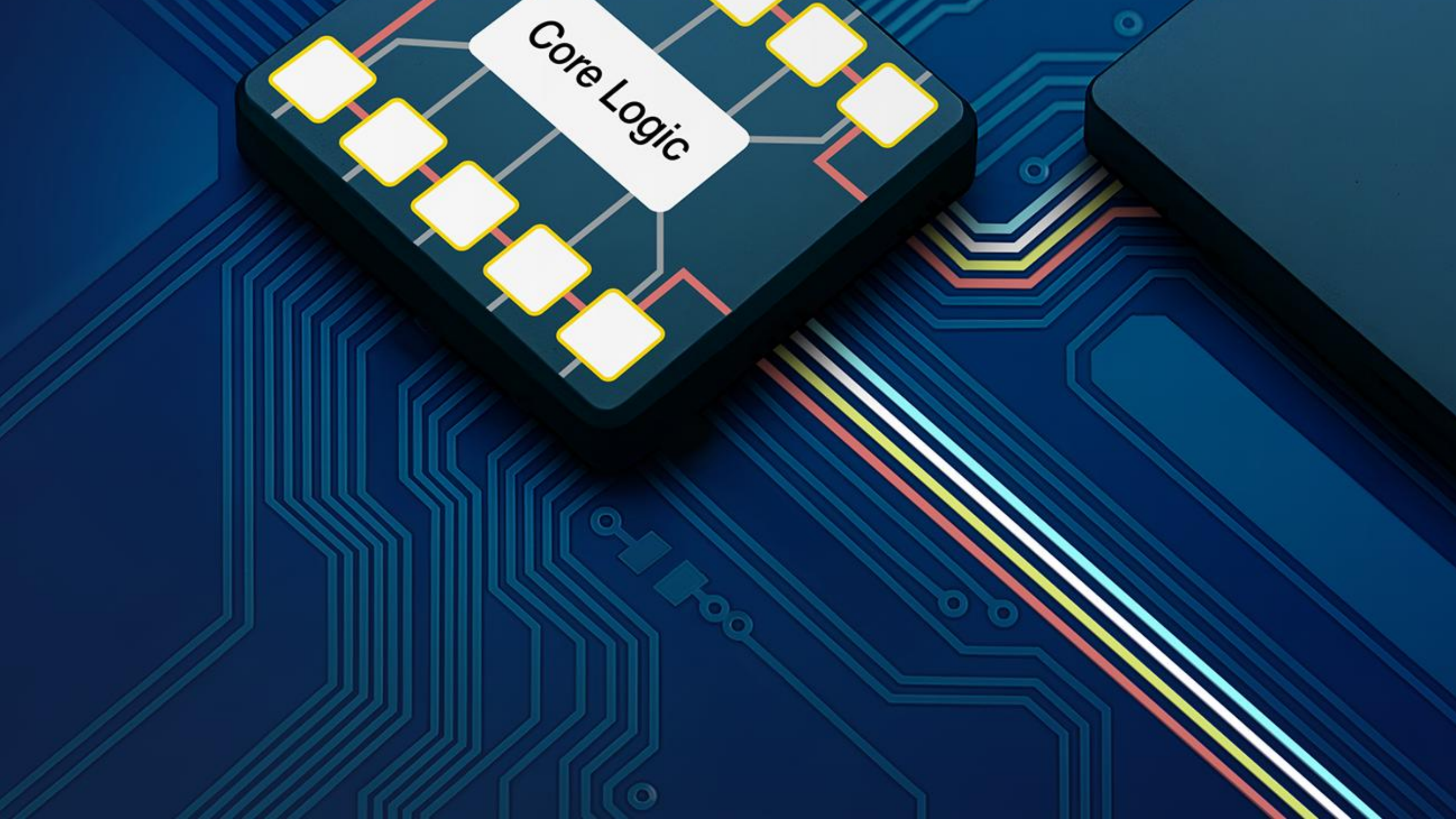
Capture data on its input

Update data onto its output

Serially scan data to neighbouring cells

Behave transparently



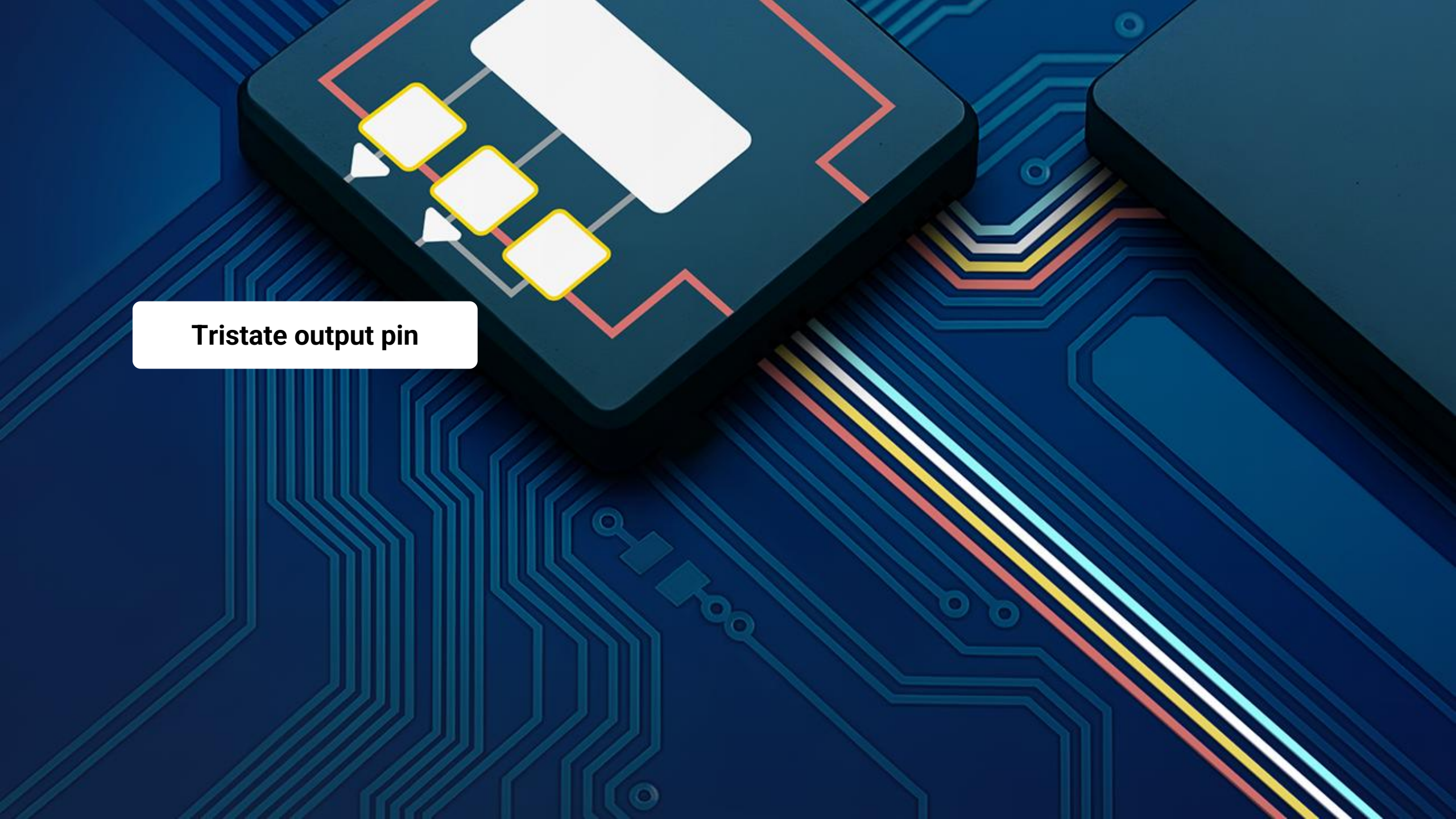




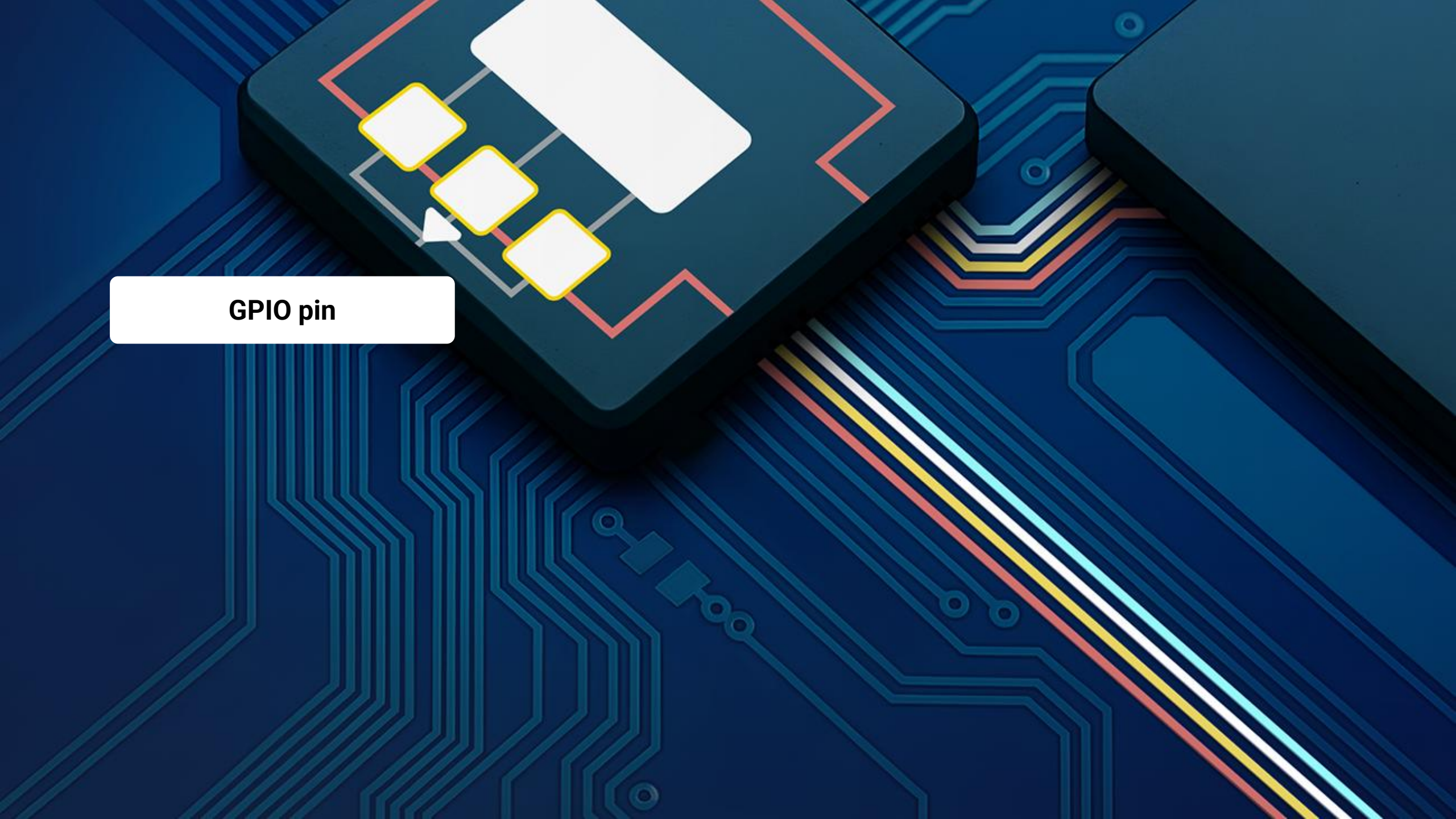
The image shows a top-down view of a microcontroller chip mounted on a blue printed circuit board (PCB). The chip is dark blue with a white rectangular label in the center. Along one edge of the chip, there are three yellow-outlined diamond shapes, each representing a pin. White arrows point from the text labels to these pins. The PCB features a complex pattern of blue, red, and yellow traces. A multi-colored ribbon cable (red, yellow, white, cyan) is connected to the board on the right side.

Output only pin

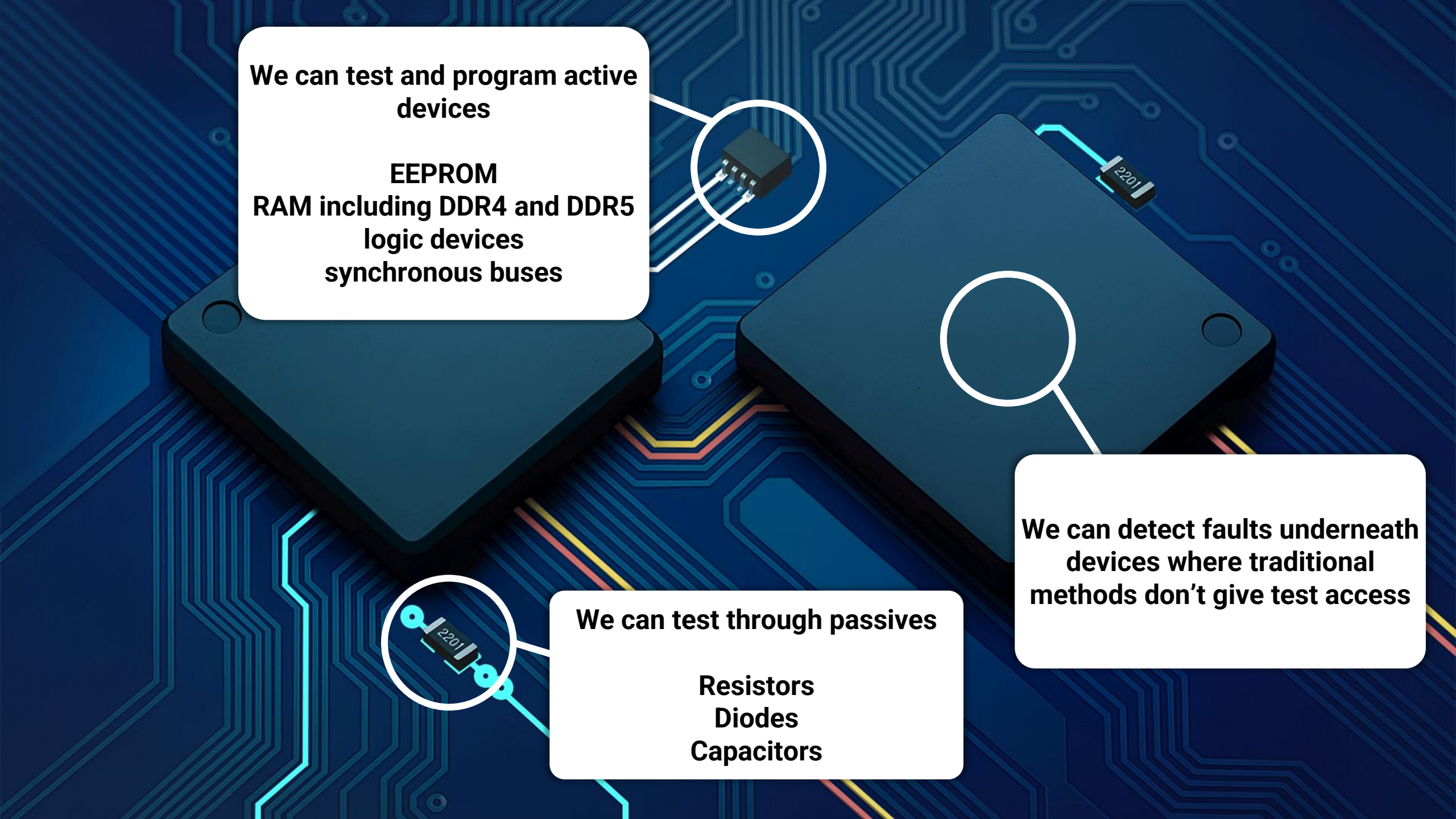
Input only pin

The image features a dark blue microcontroller chip with a white rectangular label on its top surface. Three yellow diamond-shaped pins are shown on the left side of the chip, each with a small white triangle pointing towards it. The chip is set against a background of a blue circuit board with intricate white and yellow circuit traces. A white text box with a black border is positioned to the left of the chip, containing the text "Tristate output pin".

Tristate output pin



GPIO pin



We can test and program active devices

**EEPROM
RAM including DDR4 and DDR5
logic devices
synchronous buses**

We can test through passives

**Resistors
Diodes
Capacitors**

We can detect faults underneath devices where traditional methods don't give test access

This is defined by the Boundary Scan Description Language (BSDL)

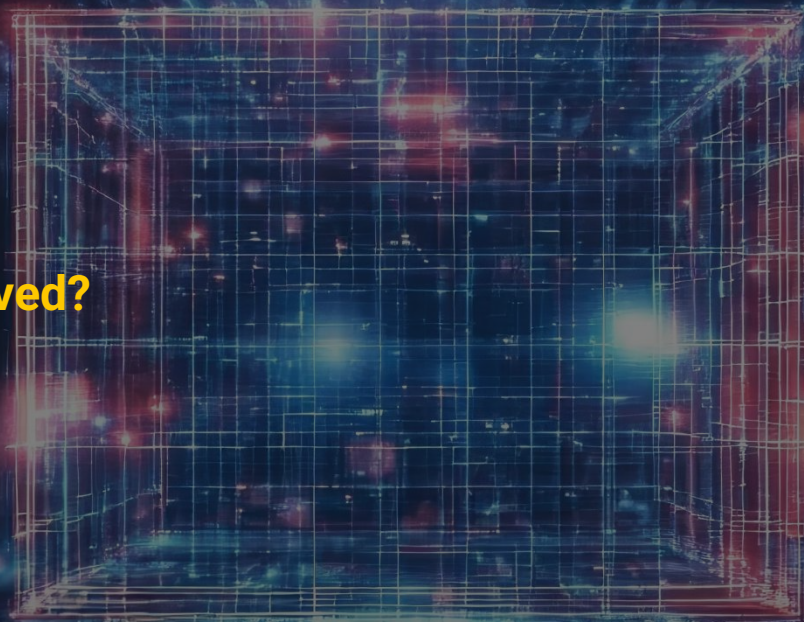
**Port description
Use statements
Component conformance to IEEE 1149.X standards
Pin mappings
Scan port identification and TCK max frequency
Compliance description
Instruction register definition
ID code definition
Boundary scan register definition**

Get BSDL files from your chip vendors



Products

What Problems Need To Be Solved?





FTDI Support

- No** Additional hardware required
- 1** JTAG Controller
- 1** TAP
- Up to 12** GPIO on Pins
- Up to 30 MHz** TCK Frequencies
- USB** Connection



XJLink2

- +5 V** Voltage Protection
- 1** JTAG Controller
- 4** TAPs
- 18** GPIO on Pins
- 2** Voltage Banks
- 2** Dedicated GND pins
- ✓ Up to 166 MHz TCK Frequencies
- ✓ Configurable Voltage
- ✓ Frequency Measurements
- ✓ Voltage Measurements
- ✓ Automatic Signal Skew Control
- Button to Start Tests
- Visual Indication of Test Status

Connection

USB

XRL-0010

PXI

RXX-0030

Keysight – i3070

AGS-0060

SPEA – 3030

SPS-0061



XJQuad

- +5 V** Voltage Protection
- 4** JTAG Controllers
- 4** TAPs per JTAG Controller
- 18** GPIO on Pins per Controller
- 2** Voltage Banks per Controller
- 2** Dedicated GND pins per Controller
- ✓ Up to 166 MHz TCK Frequencies
- ✓ Configurable Voltage
- ✓ Frequency Measurements
- ✓ Voltage Measurements
- ✓ Automatic Signal Skew Control
- ✓ Button to Start Tests
- ✓ Visual Indication of Test Status

Connection

USB

XQS-0040

ENHANCED ROBUSTNESS



XJLink-PF20

- ±30 V** Voltage Protection
- 1** JTAG Controller
- 4** TAPs
- 20** GPIO on Pins
- 2** Voltage Banks
- 20** Dedicated GND pins
- ✓ Up to 166 MHz TCK Frequencies
- ✓ Configurable Voltage
- ✓ Frequency Measurements
- ✓ Voltage Measurements
- ✓ Automatic Signal Skew Control
- ✗ Button to Start Tests
- ✓ Visual Indication of Test Status
- ✓ Mounting Kits Available

Connection

USB

XPF-0020

ENHANCED ROBUSTNESS



XJLink-PF40

- ±30 V** Voltage Protection
- 1** JTAG Controller
- 8** TAPs
- 40** GPIO on Pins
- 4** Voltage Banks
- 40** Dedicated GND pins
- ✓ Up to 166 MHz TCK Frequencies
- ✓ Configurable Voltage
- ✓ Frequency Measurements
- ✓ Voltage Measurements
- ✓ Automatic Signal Skew Control
- ✗ Button to Start Tests
- ✓ Visual Indication of Test Status
- ✓ Mounting Kits Available

Connection

USB

XPF-0040

Test



XJRunner

Run-time Manufacturing Test &
Programming Environment

RUN-0010

- ✓ Execute Tests
- ✓ Short, open faults
- ✓ Automated connection test
- ✓ Parallel testing with auxiliary controllers
- ✓ JTAG chain debugger
- ✓ Layout viewer
- ✓ Schematic viewer
- ✓ Log files
- ✓ Fault dictionaries
- ✓ LabVIEW / TestStand integration

OPTIONAL



XJAnalyser



Network Licensing



XJDeveloper

IDE for Test & Programming
Development & Debug

DEV-0010

- ✓ Develop Test Projects
- ✓ Intelligent project setup
- ✓ Multi-board setups
- ✓ Huge test library of devices
- ✓ Hundreds of supported netlist formats
- ✓ Powerful XJEase scripting
- ✓ Integrated test debugger
- ✓ Test coverage reports

INCLUDED MODULE



XJRunner
Run-time manufacturing test & program

OPTIONAL



XJAnalyser



XJFlash



Network Licensing

BEST VALUE



XJDeveloper Plus

Extended IDE for Test & Programming
Development & Debug

DEV-0011

- ✓ Develop Test Projects
- ✓ Intelligent project setup
- ✓ Multi-board setups
- ✓ Huge test library of devices
- ✓ Hundreds of supported netlist formats
- ✓ Powerful XJEase scripting
- ✓ Integrated test debugger
- ✓ Test coverage reports

ALL MODULES INCLUDED



XJRunner
Run-time manufacturing test & program



XJAnalyser
Real-time graphical board debug



XJFlash
Industry-leading fast flash programmer

OPTIONAL



Network Licensing

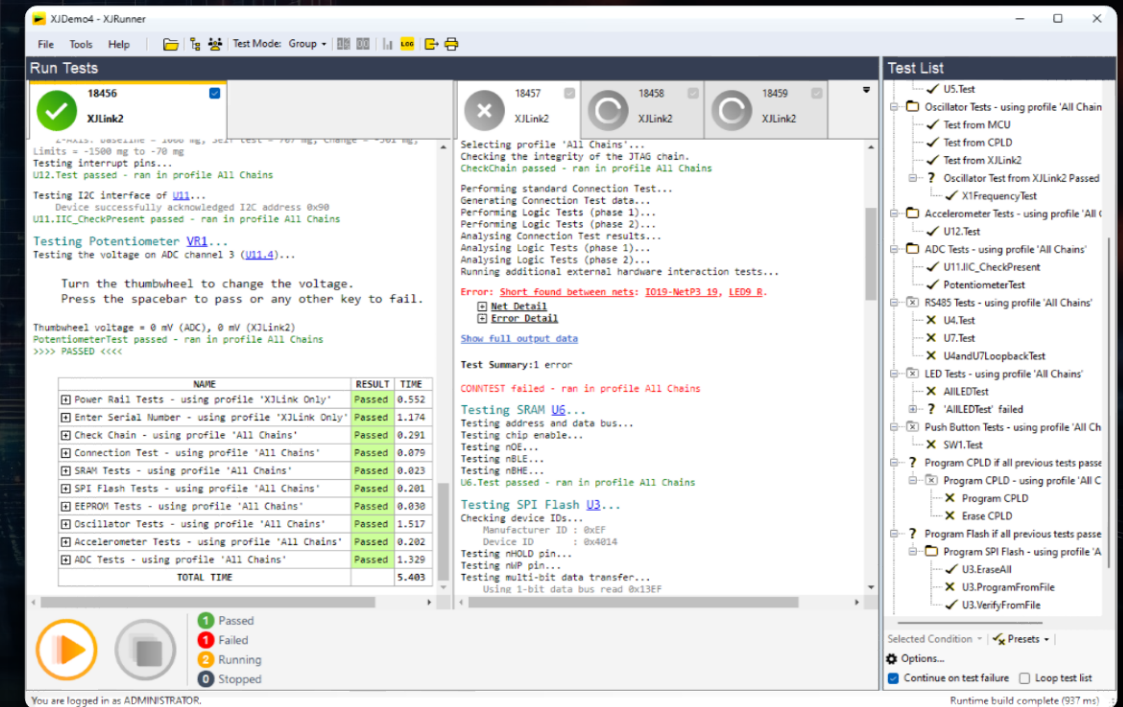


XJRunner

Run XJTAG tests in manufacturing

Features:

- Simple interface for running boundary scan projects
- Test and program boards from a single tool
- Powerful diagnostic features
- Log files for QA
- Serial number handling
- User management for tracking and administration
- Built-in viewers:
 - Layout Viewer
 - Schematic Viewer
- Easy integration with other test executive software



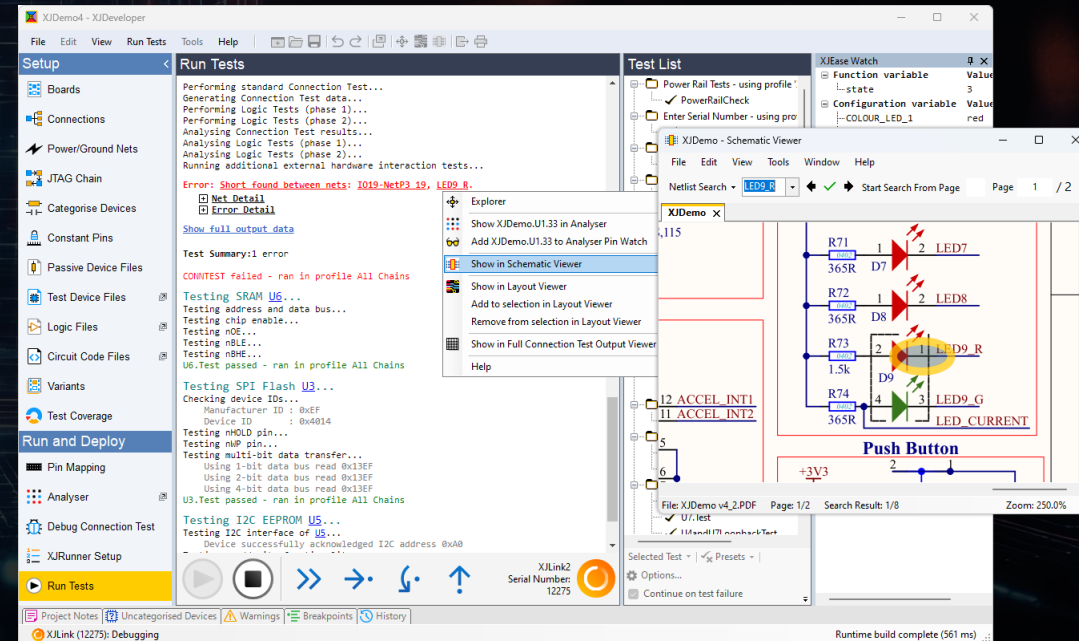


XJDeveloper

Create tests for your PCB assembly

Features:

- Describe the circuit to be tested with Netlist/ODB++, PDF Schematics, BoM and BSDL files
- Huge, maintained library of ready-to-use models for non-JTAG devices
- Review test coverage before producing or receiving hardware
- Debug tests when first hardware is received
- Test and explore prototype boards with built-in:
 - XJRunner
 - Layout Viewer
 - Schematic Viewer
 - Netlist Explorer



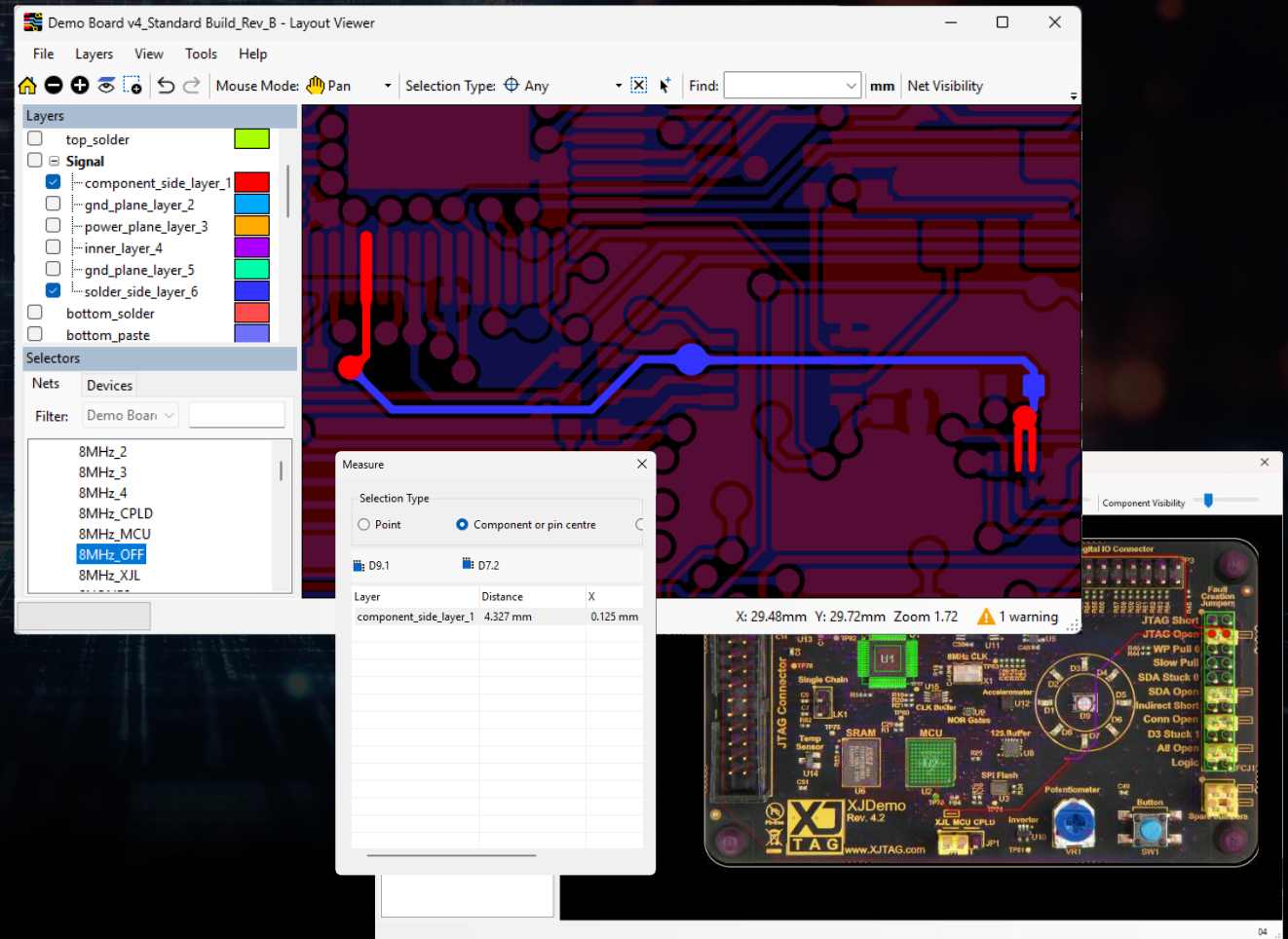


XJLayoutViewer

Free Layout Exploration Tool

Features:

- Highlight:
 - Components and devices
 - Pads
 - Nets (including across layers)
- Fully controllable layer visibility and transparency
- Rotate, flip, scale and pan views
- Snap and snapless measurements
- Powerful search tools
- Import board pictures
- ODB++ error checker



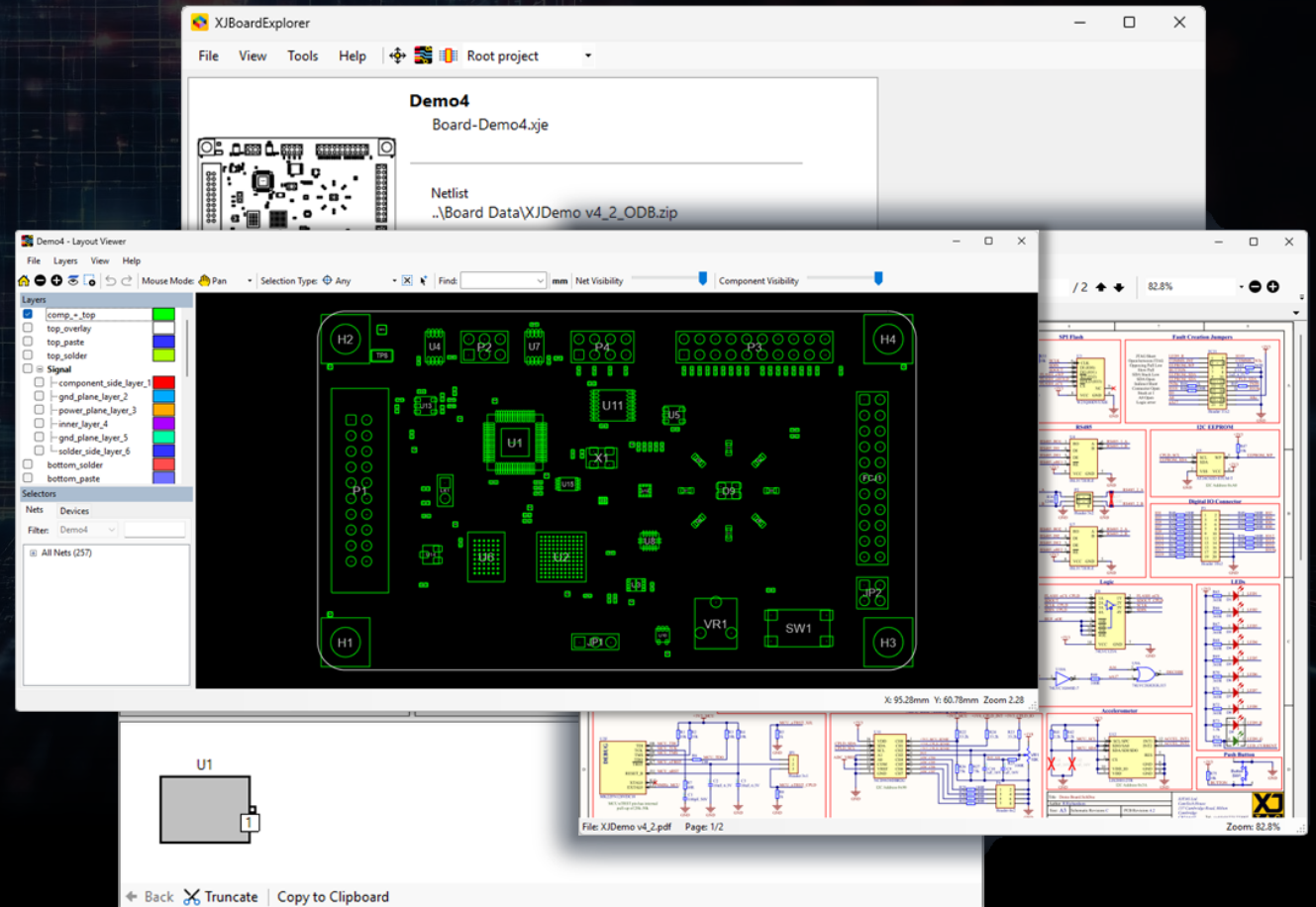


XJBoardExplorer

Explore Layouts, Netlists, Schematics & BOMs of electronics projects

Features:

- ODB++ import
- Easy-to-use, intuitive tools
- Collaborative, complex project sharing
- Layout, Netlist, Schematic and BoM support
- Fast, powerful search functionality
- Board variant handling
- Multi-board support
- Secure control of information
- Network licensed



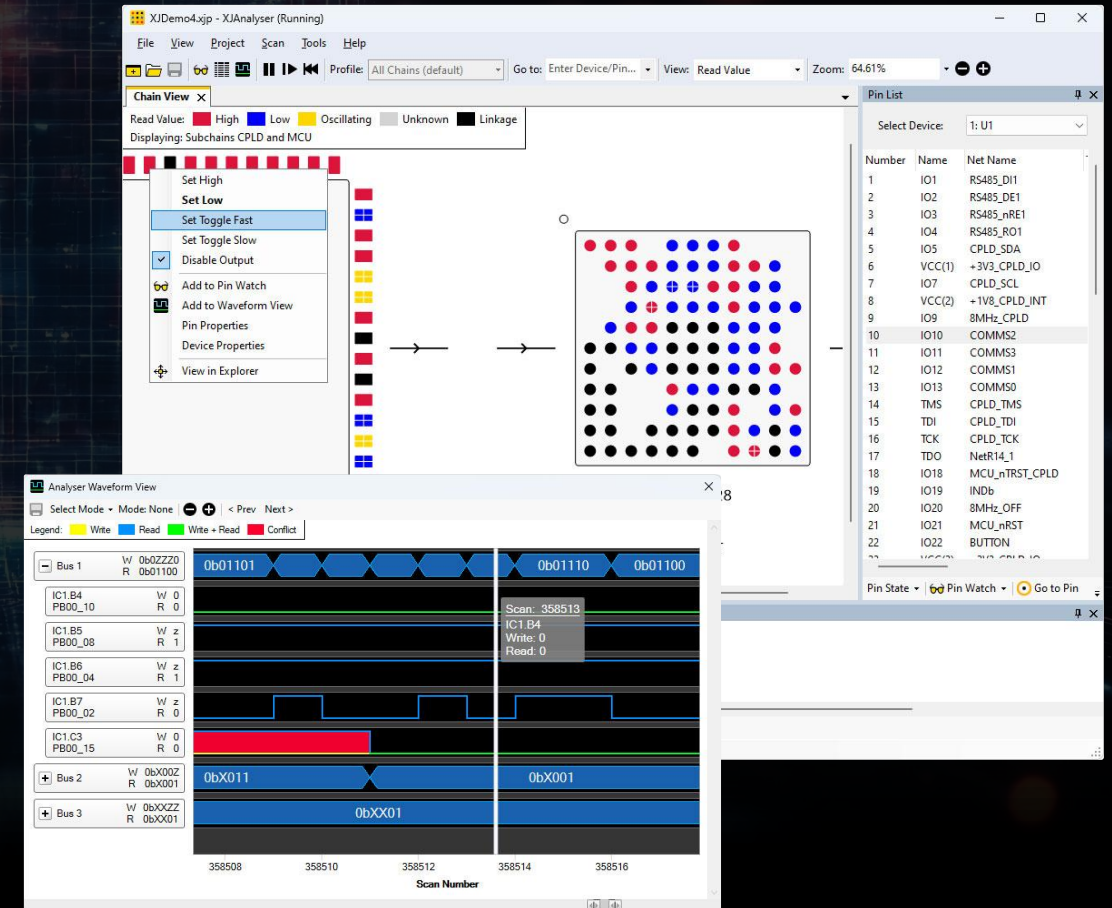


XJAnalyser

Add visual analysis and debug capabilities to your XJTAG tools

Features:

- Graphical interface for easy control and visualisation
- Direct control of JTAG enabled pins
- Golden board comparison
- SVF/STAPL programming for CPLDs, FPGAs and Xilinx configuration Flash
- Used with multimeter and oscilloscope to debug problems
- API available for easy integration with other test executives
- Built-in Waveform Viewer



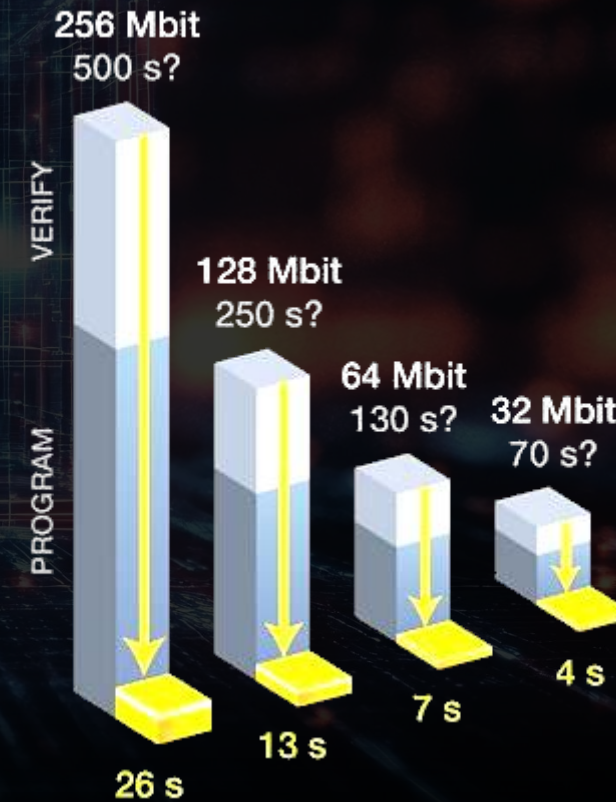


XJFlash

The fastest way to program flash

Features:

- FPGA-based ultra-fast flash programming
- Advanced and innovative method for In-System Programming (ISP) of flash devices through JTAG
- Up to 50x faster than conventional boundary scan
- Supported devices:
 - SPI, QSPI, parallel NOR flash
 - NAND flash devices available on request
 - Many Altera, Lattice, Microsemi, Xilinx FPGAs (contact us for the latest list)
 - ARM-based FPGA SoCs (e.g. Xilinx Zynq, Altera Cyclone V)
- No additional equipment
- No FPGA development required





Offers

How Can We Get Started?



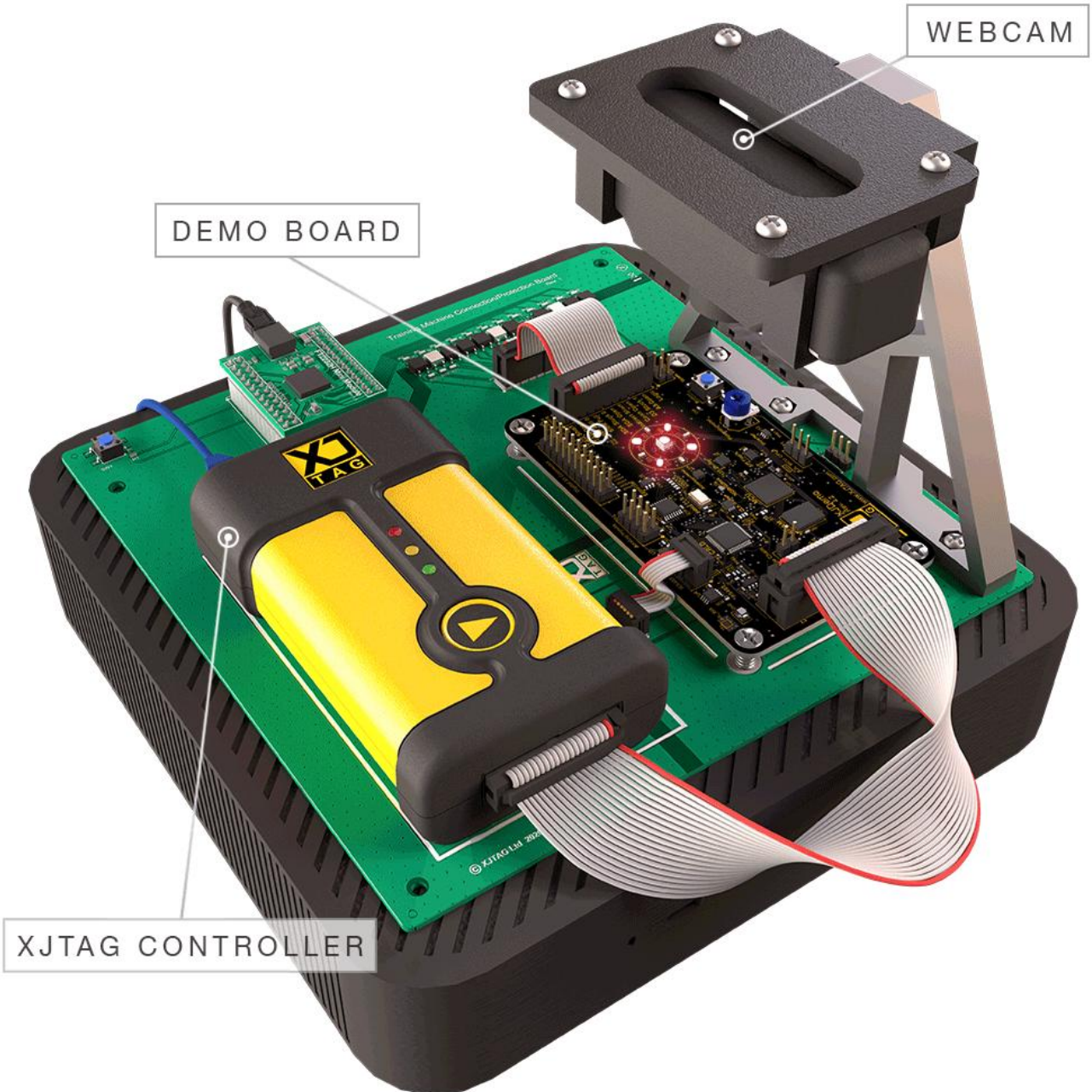
Try XJTAG Remotely

Remotely access our hardware to explore XJTAG with no limitations. Follow our step-by-step video tutorials or join a live session with one of our applications engineers. Plus, watch a collection of videos showcasing our latest features. Go to xjtag.com/workshop

Log In



Start Using Our Tools Now



Over 100 Case Studies





Thank you

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